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<b>Application Number</b>	09/531,633
<b>Filing Date</b>	03-21-2000
<b>First Named Inventor</b>	Zhe Li
<b>Group Art Unit</b>	2787
<b>Examiner Name</b>	
<b>Attorney Docket Number</b>	

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Sheet 1 of 2

U.S. PATENT DOCUMENTS

[illegible]

## FOREIGN PATENT DOCUMENTS

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ED GARCIA-OTERO

6/18/03

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## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 2 of 2

### Complete If Known

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### OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials <sup>2</sup>	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
EC	8	R. E. Bryant, "Symbolic Boolean Manipulation With Ordered Binary Decision Diagrams", ACM Computing Surveys, Vol. 24, No. 3, September 1992, pp. 293-318.	
	9	J. R. Burch, V. Singhal, "Tight Integration of Combinational Verification Methods", IEEE/ACM International Conference on Computer Aided Design Digest of Technical Papers, November 1998, IEEE, Piscataway, NJ, USA, pp. 570-576.	
	10	C. A. J. van Eijk, "A BDD Based Verification Method for Large Synthesized Circuits", INTEGRATION, the VLSI Journal, Vol. 23, No. 2, November 1997, pp. 131-149.	
	11	J. Jain et al., "A Survey of Techniques for Formal Verification of Combinational Circuits", Proceedings of IEEE International Conference on Computer Design: VLSI in Computers and Processors, October 1997, IEEE, Piscataway, NJ, USA, pp. 445-454.	
	12	J. P. Marques-Silva, K. A. Sakallah, "Boolean Satisfiability in Electronic Design Automation", Proceedings of 37th Design Automation Conference, June 2000, IEEE, Piscataway, NJ, USA, pp. 657-662.	
EG	13	S. Woods, G. Casinovi, "Efficient Solution of Systems of Boolean Equations", IEEE/ACM International Conference on Computer Aided Design Digest of Technical Papers, November 1998, IEEE, Piscataway, NJ, USA.	

Examiner  
Signature

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Date

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